A 3-WATT X-BAND MONOLITHIC VARIABLE GAIN AMPLIFIER

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ABSTRACT

The design and performance of a monolithic dual-gate GaAs FET 3-watt X-Band amplifier are discussed. The two-stage amplifier demonstrates 13 dB gain and over 20 percent power-added efficiency. Both large-signal and small-signal gain can be varied 20 dB while exhibiting less than +/- 6 degrees insertion phase variation.

INTRODUCTION

Dual-gate FET (DGFET) amplifiers for applications requiring variable gain while maintaining constant insertion phase have been previously reported [1,2]. However, many radar applications require higher output power levels with high efficiency due to limited prime power and heat transfer availability. This paper presents a monolithic amplifier design which has been structured for high power and low phase variation over gain control using a gate-2 impedance termination as described in [3].

DUAL-GATE FET GEOMETRY

The geometry of an 1800 micron DGFET [3] was modified and the device model scaled to obtain the 2000 micron FET shown in Figure 1 which was used in the MMIC. It consists of twenty 100 micron wide gate fingers with 25 micron gate-to-gate spacing. The two gate feeds are flanked by three source vias and the two drain feeds are flanked by three gate-2 capacitors positioned directly over vias. The gate-2 capacitance was chosen to series resonate at 12 GHz with the via and connecting inductance to avoid an inductive gate-2 termination which would cause poor phase performance during gain control. Differential mode oscillations are inhibited by the parallel connection of gate-1, gate-2 and drain contacts which are easily extended to additional parallel FETs.

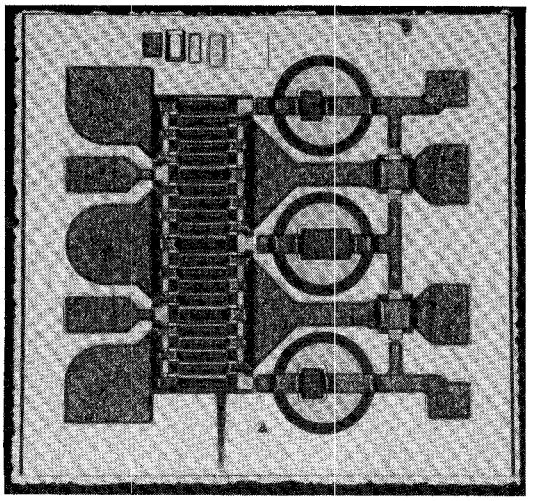

Figure 1. 2000 Micron Dual-Gate FET.

CIRCUIT DESIGN

A two-stage design was chosen rather than a single stage amplifier primarily for its inherent lower gate impedance transformation ratios. The FET cell described above is used in the first stage and four identical cells used in parallel for the second stage. The total on-chip gate periphery is 10 mm. All matching networks are organized into binary tree structures to preserve equal amplitude and in-phase power dividing and combining. A composite schematic diagram is shown in Figure 2. The output matching network is a low-pass transformer with a three element high-pass section embedded in it to inject drain bias. The widths of the transmission lines which carry drain current are scaled to 25 microns per mm of FET periphery. This design guideline maintains current density below 2.6 X 10^5 amps/cm^2 at Idss to minimize metal migration and voltage drop. The

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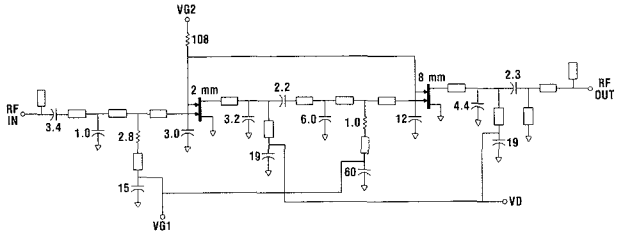

Figure 2. 3 Watt MMIC Schematic Diagram (Values in PF and Ohms).

input and interstage matching networks employ a lossy match for gain flattening, lower impedance matching Q, convenient gate bias injection, and low frequency stability. Initial values for this gate "de-Q-ing" portion of the network were chosen as follows: the gate capacitance was series resonated at 12 GHz and a series RL placed in shunt with resistance equal to the gate resistance and reactance at 12 GHz three times the resistance value. The remainder of the input and interstage network was designed as a low-pass impedance transformer.

The MMIC, shown in Figure 3, is 6.6 X 3.8 X 0.1 mm. On-chip connections provide gate and drain bias for both stages simultaneously. In a typical radar application, the drain bias is modulated while the gate-2 bias may be positive. This forward biases gate-2 during the off portion of the period, resulting in gate current which is both wasteful as overhead current and can be a reliability concern. Therefore, on-chip current limiting resistors are included in the gate-2 bias line. Series conductance scaled to 1 mmho per mm of supplied gate periphery limits the current acceptably while not degrading rise time associated with the gate-2 circuit capacitance. Figure 4 shows the backside of the MMIC and the via locations. There are a total of 48 vias: 13 source grounds, 13 gate-2

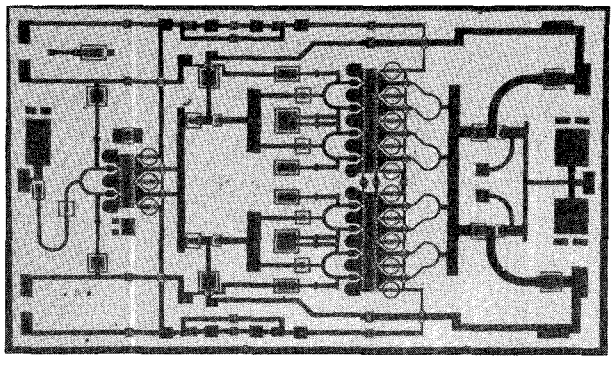

Figure 3. Monolithic Power Amplifier.

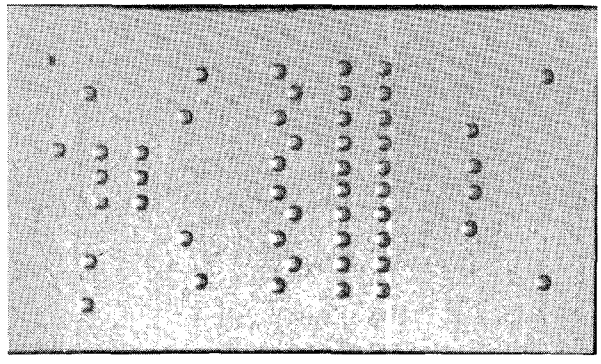

Figure 4. MMIC Backside.

capacitor grounds, 12 bypass capacitor grounds and 10 shunt MIM tuning capacitor grounds. The total MIM capacitance is 150 pF.

RF PERFORMANCE

Twelve slices have been evaluated and the performance of a typical chip is shown in Figures 5 through 10. As shown in Figure 5, the output power is greater than 3 watts with over 20 % power-added efficiency with a 9 volt, 2.0 uSec, 50 % duty cycle drain pulse. Large-signal gain is 13 dB. Figures 8 and 9 show the relative insertion phase variation at 8 frequencies for 20 dB of large-signal and small-signal gain control. In both cases, the phase variation is less than +/- 6 degrees. Both amplifier stages are controlled with a single gate-2 control line which is varied from + 2.5 to -2.5 volts. Finally, Figure 10 shows the compression characteristic at the same 8 frequencies for output power, relative insertion phase and efficiency.

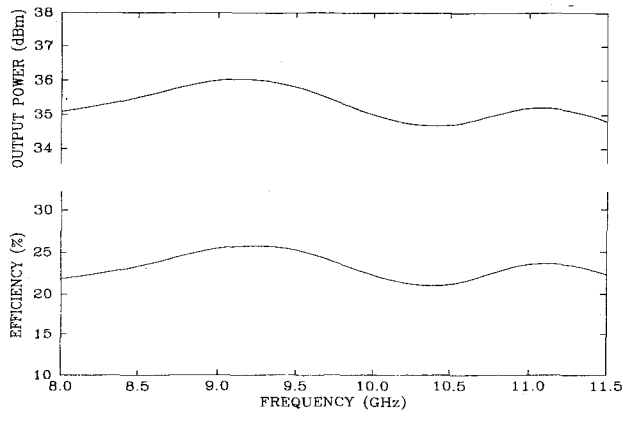

Figure 5. MMIC Output Power and Power Added Efficiency.

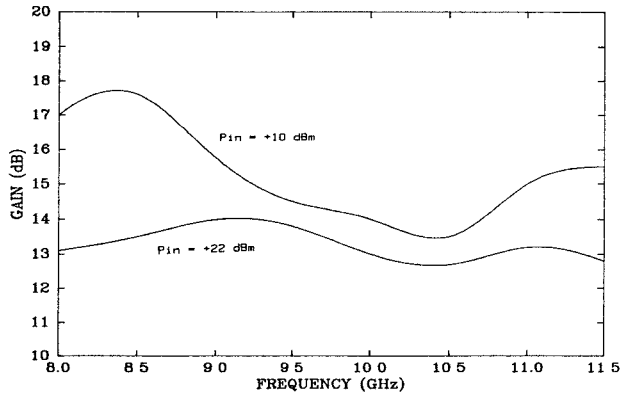

Figure 6. MMIC Gain.

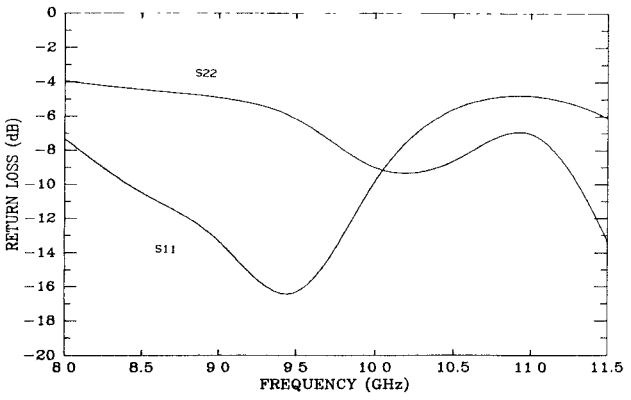

Figure 7. MMIC Input and Output Return Loss.

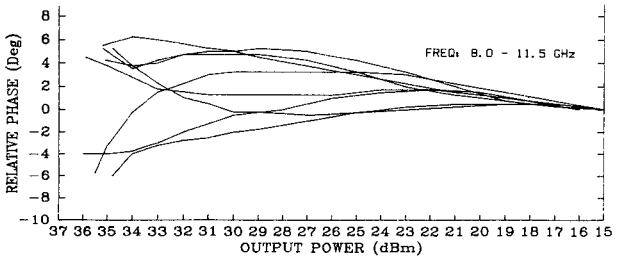

Figure 8. Large-Signal Phase Variation with Gain Control.

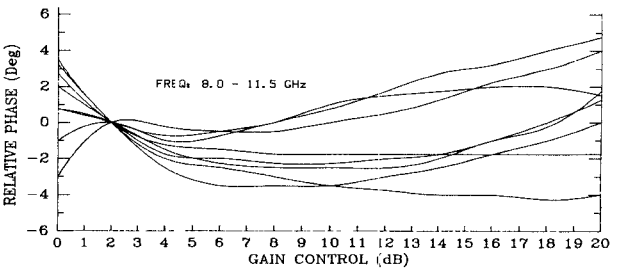

Figure 9. Small-Signal Phase Variation with Gain Control.

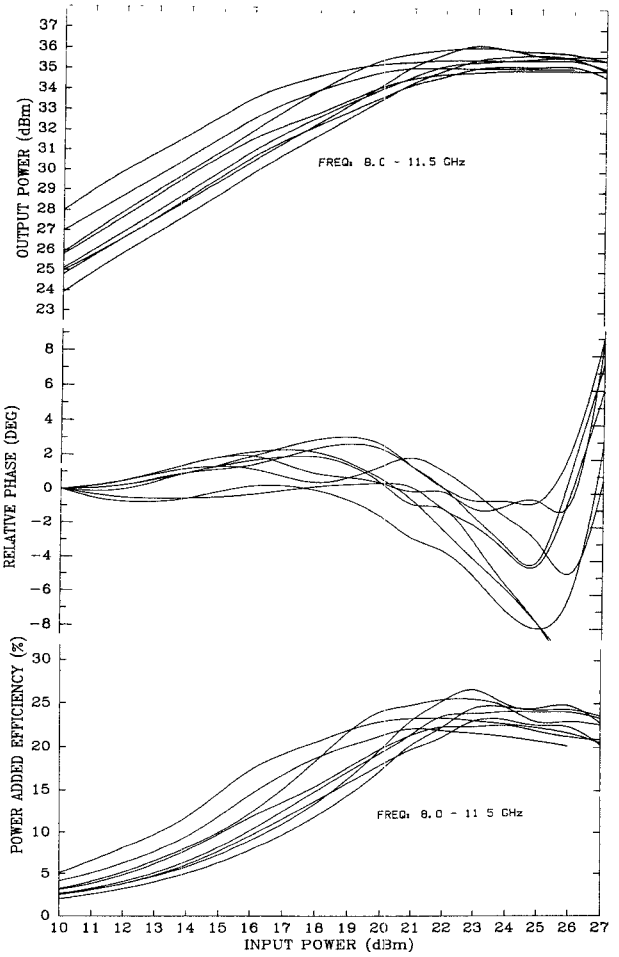

Figure 10. MMIC Compression Characteristic.

CONCLUSION

A two-stage 3-watt monolithic variable gain amplifer has demonstrated 13 dB gain and over 20 % efficiency with low insertion phase variations over a 30% bandwidth. The successful performance has established confidence in the utility of shunt in-line MIM tuning capacitors and large binary tree structures for on-chip power combining. In addition, this design has established confidence in the producibility of a large and fairly complex MMIC with substantial gate periphery, relatively large total MIM capacitance and many vias.

REFERENCE

[1] B.M. Kim, H.Q. Tserng, and P. Saunier, *"GaAs Dual-Gate FET for Operation up to K-Band,"* IEEE Trans. Microwave Theory and Tech., Vol. MTT-32, no. 3, March 1984.

[2] P. Saunier, H.Q. Tserng, B. Kim and G H. Westphal, *"Monolithic GaAs Dual-Gate FET Variable Power Amplifier Module,"* IEEE 1985 Microwave and Millimeter-wave Monolithic Circuits Symposium Digest of Papers, pp. 1-3.

[3] D.M. Drury, D.C. Zimmermann, and D.E. Zimmerman, *"A Dual-gate FET Constant Phase Variable Power Amplifier,"* 1985 IEEE-MTT-S International Microwave Symposium Digest, pp. 219-222.